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(54) Multilayer package.

(57) The present invention provides a multilayer ceramic package, which comprises a conductive layer, formed like a square film (11), applying a power voltage V_{DD} or a ground voltage V_{SS} to a semiconductor device, and having a square hole in its central portion, a plurality of inner leads connected to the conductive layer at the inner portion of the conductive layer, and a plurality of outer leads connected to the conductive layer at the outer portion of the conductive layer, wherein if a first contact point between the inner lead and the conductive layer, a second contact point between the outer lead and conductive layer, a distance between adjacent two first contact points is C_1, a distance between adjacent two second contact points is C_2, a shortest distance from the first contact point to the second con-tact point is h, both C_1/h and C_2/h are 3/8 or less.

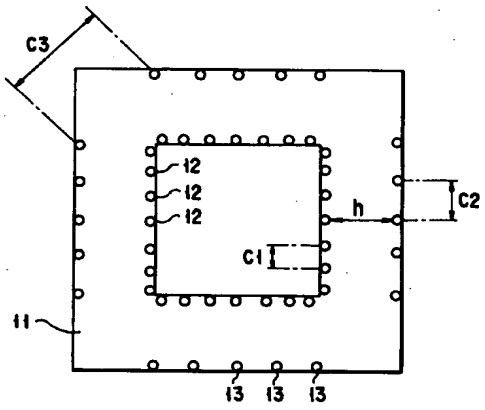

FIG. 4A

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The present invention relates to improvement of a conductive layer for a power voltage V_{DD} or a ground voltage V_{SS} using a multilayer plastic package and a multilayer ceramic package such as a pin grid array package (PGA).

Conventionally, in a multilayer ceramic package such as a pin grid array package (PGA), a conductive layer (hereinafter called simply as conductive layer) for supplying a power voltage V_{DD} or a ground voltage V_{SS} to a semiconductor device (IC chip) is structured as shown in Fig. 1.

That is, in Fig. 1, a conductive layer 11 comprises a square layer-like conductor. In the central portion of the conductive layer 11, a square hole is formed. In the end portion of the inside of the conductive layer 11, contact points 12 to be connected to an inner lead are formed. The contact points 12 are irregularly arranged due to a bonding pad formed in the inner lead. Therefore, the distance among the contact points 12 differs.

In the end portion of the outside of the conductive layer 11, contact points 13 to be connected to an outer lead for a power voltage source or a ground pin are formed. The contact points 13 are irregularly arranged due to the other outer lead for a signal pin.

Therefore, similar to the contact points 12, the distance among the contact points 13 differs.

In the conventional multilayer ceramic package, the positions and the number of the contact points 12 and 13 are determined regardless of the shape of the conductive layer 11. In other words, in conventional, neither the rule of the arranging method of the contact points 12 and 13 nor the rule of the setting method of the number of the leads exists.

In the state that no constant rule exists, if a plurality of output buffers, which are formed in the IC chip in the package, are turned on at the same time, a large current must be supplied to the IC chip during a short period of time in order to normally drive the plurality of the output buffers. In this case, in the conventional package, the current flowing in the conductive layer 11 becomes uneven, the power voltage V_{DD} or the ground voltage V_{SS} largely varies. This variation becomes the so-called simultaneous switching noise, thereby causing an erroneous operation of an input buffer or that of a logic circuit.

Fig. 2 shows a distribution of current density of the conductive layer 11 for the ground voltage V_{SS} and current is dense in an area D.

In order to eliminate the above problem, the present invention has been made, and an object of the present invention is to provide a multilayer ceramic package wherein a distribution of current density of a conductive layer for a power voltage V_{DD} or a ground voltage V_{SS} is uniformed and conductor resistance and inductance are reduced and simultaneous switching noise is also reduced, and delay of an output signal in an output buffer is reduced.

In order to attain the above object, according to the multilayer ceramic package of the present invention, a conductive layer for supplying a power voltage V_{DD} or a ground voltage V_{SS} to a semiconductor device is connected to a plurality of inner leads and a plurality of outer leads. The shape of the conductive layer is squire layer-like, and a square hole is formed in the central portion of the conductive layer. Each inner lead is connected to the conductive layer at the end portion of the inside of the conductive layer. Each outer lead may be connected to the conductive layer at the portion other than the end portion of the outside of the conductive layer. In a case where a distance between the inner lead and a first contact point of the conductive layer is C_1, and a distance between the outer lead and a second contact point of the conductive layer is C_2, and the shortest distance from the first contact point to the second contact point is h, the distance between adjacent two contact points of the inner lead is 3/8 or less of the shortest distance from one contact point of the inner lead to one contact point of the outer lead. Similarly, "the distance between adjacent two contact points of the outer lead is 3/8 or less of the shortest distance from one contact point of the inner lead to one contact point of the outer lead.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a plane view of a conventional conductive layer;

Fig. 2 is a view showing a distribution of current density in the conductive layer of Fig. 1;

Fig. 3 shows a relationship between the number of leads and inductance;

Figs. 4A and 4B are plane views showing the position of contact points between a conductive layer and a lead of a multilayer package of the present invention;

Fig. 5 is a view showing a distribution of current density in the conductive layer of Fig. 4A;

Figs. 6A to 16B and Figs. 17 and 18 are plane views each showing the position of contact points between the conductive layer and the lead of the multilayer package of the present invention;

Fig. 19 is an exploded perspective view showing a multilayer ceramic package according to one embodiment of the present invention;

Fig. 20 is a cross sectional view of the multilayer ceramic package of Fig. 19;

Fig. 21 is a plane view showing a multilayer plastic package according to the other embodiment of the present invention;

Fig. 22 is a cross sectional view of the multilayer plastic package of Fig. 21;

Figs. 23 and 24 are plane views showing the multilayer plastic package according to the other embodiment of the present invention; and

Fig. 25 is a cross sectional view of the multilayer plastic package of Figs. 23 and 24.

An embodiment of the present invention will be explained with reference to the drawings.

Fig. 19 is an exploded perspective view showing a multilayer ceramic package according to one embodiment of the present invention. Fig. 20 is a cross sectional view of the multilayer ceramic package of Fig. 19. The package is formed of seven layers A to G. Each layer comprises plate-like ceramic substrates 1a to 1g, serving as insulating materials, and conductive layers 2a to 2g formed on the ceramic substrates 1a to 1g.

The surface of layer A forms a part of the surface of the package. A number of via holes 3 are formed in the substrate 1a. Outer leads 4 such as a signal pin, a power pin, a ground pin are formed on the conductive layers 2a.

Layers B and D are signal wiring layers.

Conductive layers 2b and 2d having a predetermined wire pattern are formed on the substrates 1b and 1d. The via holes 3 are formed in the substrates 1b and 1d. The conductive layers 2b and 2d are formed in and on the corresponding via holes 3.

Layer C is a conductive layer for ground voltage V_{SS}. The conductive layer 2c is formed on the substrate 1c. The conductive layer 2c is shaped square and has a square hole in its central portion. The via holes 3 are formed in the substrate 1c, and the conductive layer 2c is formed on the via holes. A contact point 12 to be in contact with an inner lead 5 (bonding wire) is formed at the end portion of the inside of the conductive layer 2c. A contact point 13 to be in contact with an outer lead 4 (ground pin) is formed at the end portion of the outside of the conductive layer 2c. The positions of the contact points 12 and 13 are explained later.

Layer E is a conductive layer for power voltage V_{DD}. The conductive layer 2e is formed on the substrate 1e. The conductive layer 2e is shaped square and has a square hole in its central portion. The via holes 3 are formed in the substrate 1e, and the conductive layer 2e is formed on the via holes. A contact point to be in contact with an inner lead is formed at the end portion of the inside of the conductive layer 2e. A contact point 13 to be in contact with an outer lead is formed at the end portion of the outside of the conductive layer 2e. The positions of the contact points 12 and 13 are explained later.

Layer F is is a conductive layer for power voltage V_{DD}. The structure layer F is substantially the same the structure of layer E. The different point between layers E and F is that the conductive layer 2f is shaped square. Also, an IC chip 14 is mounted on the central portion of the conductive layer 2f.

Layer G is is a conductive layer for ground voltage V_{SS}. The structure layer G is substantially the same the structure of layer C. The different point between layers G and C is that the conductive layer 2g is shaped square and the surface of the substrate 1g forms the part of the surface of the package.

Fig. 21 is a plane view showing a multilayer plastic package according to the other embodiment of the present invention. Fig. 22 is a cross sectional view of the multilayer plastic package of Fig. 21. The package is formed of two layers A and B. The layer A is a conductive layer for power voltage V_{DD} or ground voltage V_{SS}, and the layer B is mainly used as a signal wiring layer.

The layer A comprises four plate-like conductive materials 20. The IC chip 14 is surrounded by these conductive materials 20. Each conductive material 20 may be insulated from each other or short-circuited. The contact point 12 to be in contact with the inner lead 5 (bonding wire) is formed at the end portion of the IC chip side (inside) of the conductive material 20. The contact point 13 to be in contact with the outer lead 4 is formed at the end portion of the outside of the conductive material 20. The positions of the contact points 12 and 13 are explained later.

Figs. 23 and 24 are plane views showing a multilayer plastic package according to the other embodiment of the present invention. Fig. 25 is a cross sectional view of the multilayer plastic package of Figs. 23 and 24. The package is formed of three layers A, B, and C. The layer A is a lead layer for signal or power voltage V_{DD}/ground voltage V_{SS}. The layers B and C are conductive layers for power voltage V_{DD} or ground voltage V_{SS}.

The layer B comprises a plate-like conductive material 20b having a square hole in its central portion. The IC chip 14 is positioned at the central portion of the hole. The contact point 12 to be in contact with the inner lead 5 (bonding wire) is formed at the end portion of the IC chip side (inside) of the conductive material 20b. The contact point 13 to be in contact with the outer lead 4 is formed at the end portion of the outside of the conductive material 20b. The positions of the contact points 12 and 13 are explained later.

The layer C comprises a square plate-like conductive material 20c. The IC chip 14 is positioned at the central portion of the conductive material 20c. The contact point 12 to be in contact with the inner lead 5 (bonding wire) is formed at the end portion of the IC chip side (inside) of the conductive material 20c. The contact point 13 to be in contact with the outer lead 4 is formed at the end portion of the outside of the conductive material 20c. The positions of the contact points 12 and 13 are explained later.

The following will explain the positions of the contact points 12 and 13 on the conductive layer for power voltage V_{DD} or ground voltage V_{SS} of the multilayer ceramic package, and the positions of the contact points 12 and 13 on the conductive layer for power voltage V_{DD} and ground voltage V_{SS} of the multilayer plastic package.

Increase in simultaneous switching noise results from increase in inductance of the conductor for the power voltage V_{DD} or the ground voltage V_{SS} of the multilayer ceramic package. As shown in Fig. 1, according to the conventional package, the contact point 12 between the conductive layer 11 and the inner lead and the contact point 13 between the conductive layer 11 and the outer lead are irregularly determined, respectively. Due to this, the distribution of current density in the conductive layer 11 becomes uneven, and inductance of the conductive layer 11 increases.

The present invention provides a multilayer ceramic package wherein distribution of current density in the conductive layer is substantially uniformed. In other words, according to the present invention, attention is paid to the point that conductive resistance and inductance becomes minimum when distribution of current density in the conductive layer is uniformed.

Therefore, in the present invention, distribution of current density in the conductive layer is set to be substantially uniformed, thereby the simultaneous switching noise is reduced.

In order to equalize the distribution of current density in the conductive layer, first, a relationship between the number of leads and inductance must be reviewed. Fig. 3 shows the relationship between the number of leads and inductance. As is obvious from Fig. 3, inductance reduces as the number of leads increases (the distances among leads are narrowed), and inductance reaches close to a logical value. The following conditions can be obtained from the analyzed result of the distribution of current density.

A) First Condition

"A distance from one contact point of the inner lead to one contact point of the outer lead is the shortest distance." That is, the distance from one contact point of the inner lead to one contact point of the outer lead is set to be as short as possible, so that a current passage is made short. This condition is derived from the reason that conductor resistance of the conductive layer and self-inductance are increased in proportion to the distance (length of the current passage) from one contact point of the inner lead to one contact point of the outer lead.

B) Second Condition

"The number of contact points of the inner lead is equal to that of the contact points of the outer lead, and these points are regularly arranged."

That is, the contact points of the inner lead and those of the outer lead are symmetically arranged. This condition is derived from the reason that the phenomenon of the local concentration of the current distribution and that of the ununiformity of the current distribution are generated by the point that the contact points are arranged at random.

C) Third Condition

"The distance between adjacent two first contact points is 3/8 or less of the shortest distance from one first contact point to one second contact point, wherein each first contact point is between the conductive layer and the inner lead.

Similarly, "the distance between adjacent two second contact points is 3/8 or less of the shortest distance from one first contact point to one second contact point, wherein each second contact points is between the conductive layer and the outer lead.

The above condition is derived from the reason that if each current density of the currents flowing from adjacent two contact points of the inner lead becomes half at a portion where the currents cross, the substantially equal distribution of current density can be obtained in the conductive layer.

The portion where the current density becomes half can be obtained by an electric image method from the following equation (1).

$$W = \{(4 \times h^6)^{1/3} - h^2\}^{1/2} \approx 0.766 \cdot h \approx (3/4) \cdot h \quad (1)$$

wherein W a distance between adjacent two contact points, h is the shortest distance from one contact point of the inner lead to one contact point of the outer lead.

According to the above condition, the distribution of current density at the intermediate point between the contact point of the inner lead and that of the outer lead is uniformed.

The above condition is derived from the results of the measurement and analysis. That is, the distribution of current density in the conductive layer is uniformed when the area where current uniformly flows amounts to more than a half area of the whole conductive layer.

The space of the contact points to satisfy the above condition according to the electric image method is shown as the following equation (2):

$$W \leq 2 \times (3/4) \times (1/2) \times \{(1/2) \times h\} \leq (3/8) \cdot h \quad (2)$$

wherein W is a distance between the adjacent two contact points, h is the shortest distance from one contact point of the inner lead to one contact point of the outer lead.

According to the multilayer ceramic package satisfying at least one of the above first to fourth conditions, the distribution of current density in the conductive layer for the power voltage V_{DD} or ground voltage V_{SS} can be uniformed. Thereby, conductor resistance of the conductive layer and inductance can be reduced and simultaneous switching noise can be also reduced.

In the case where the present invention is applied to the ceramic pin grid array package, the pin pitch can be 50 mil or less and the number of pins can be 300 or more. Moreover, In the case where the present invention is applied to the ceramic flat package, the lead pitch can be 25 mil or less and the number of leads can be 300 or more.

Figs. 4A and 4B show a conductive layer of a multilayer ceramic package according to one embodiment of the present invention. In Figs. 4A and 4B, reference numeral 11 is a conductive layer, 12 is a contact point between the inner lead and the conductive layer; C_1 is a distance between the adjacent two contact points 12 (excepting corner portions). Reference numeral 13 is a contact point between the outer lead and the conductive layer and C_2 is a distance between the adjacent two contact points 13 (excepting corner portions).

The package of Fig. 4 is structured to satisfy the above first and third conditions. That is, the distance C_1 between the adjacent two contact points 12 is 3/8 or less of the shortest distance h from one contact point of the inner lead to one contact point of the outer lead. Similarly, the distance C_2 between the adjacent two contact points 13 is 3/8 or less of the shortest distance h from one contact point of the inner lead to one contact point of the outer lead.

Fig. 5 shows the distribution of current density in the conductive layer 11 of the multilayer ceramic package of Fig. 4A. In Fig. 5, D is an area where the current concentrates. As is obvious from the drawing, according to the present invention, the distribution of current density in the conductive layer 11 is more uniformed compared with the prior art. Therefore, the conductor resistance of the conductive layer and inductance can be reduced and simultaneous switching noise can be also reduced.

Figs. 6A to 18A and Figs. 6B to 18B show the multilayer ceramic packages according to the other embodiments of the present invention.

Similar to the package of Figs. 4A and 4B, the package of Figs. 6A and 6B are structured to satisfy the above condition. All contact points 13 are arranged in the portions closer to the contact points 12 at the portions, which are not end portions of the conductive layer 11, for example, within an allowable range, which is determined every package. According to this structure, the distance C_3 between the contact points 13 at the corner portions of the conductive layer 11 can be narrowed. Moreover, in addition to the same technical advantage as the package of Figs. 4A and 4B, the current passage can be shorten. Thereby, the conductor resistance of the conductive layer and inductance can be reduced and simultaneous switching noise can be also reduced.

The package of Figs. 7A and 7B is structured to satisfy all first to third conditions. More specifically, the distance C_1 between the adjacent two contact points 12 is 3/8 or less of the shortest distance h from one contact point of the inner lead to one contact point of the outer lead. Similarly, the distance C_2 between the adjacent two contact points 13 is 3/8 or less of the shortest distance h from one contact point of the inner lead to one contact point of the outer lead. The number of contact points 12 is equal to that of contact points 13.

In this package, one contact point 12 pairs with one contact point 13. The pair of contact points 12 and

13 are arranged to be opposed to each other with a shortest distance. According to this structure, in addition to the same technical advantage as the package of Figs. 4A and 4B, the potential distribution is symmetrized, so that ununiformity of the distribution of current density can be reduced. Thereby, the conductor resistance of the conductive layer and inductance can be reduced.

Similar to the package of Figs. 7A and 7B, the package of Figs. 8A and 8B is structured to satisfy all first to third conditions. The contact points 13 are arranged in the portions closer to the contact points 12 at the portions, which are not end portions of the conductive layer 11, for example, within an allowable range, which is determined every package. According to this structure, the distance C_3 between the contact points 13 at the corner portions of the conductive layer 11 can be narrowed. Moreover, in addition to the same technical advantage as the package of Figs. 7A and 7B, the current passage can be shorten. Thereby, the conductor resistance of the conductive layer and inductance can be reduced and simultaneous switching noise can be also reduced.

The package of Figs. 9A and 9B is structured to satisfy the first and third conditions. More specifically, the distance C_2 between the adjacent two contact points 13 is 3/8 or less of the shortest distance h from one contact point of the inner lead to one contact point of the outer lead. According to this structure, in addition to the same technical advantage as the package of Figs. 4A and 4B, the uniform area of the distribution of current density is enlarged. Thereby, the conductor resistance of the conductive layer and inductance can be reduced and simultaneous switching noise can be also reduced.

Similar to the package of Figs. 9A and 9B, the package of Figs. 10A and 10B is structured to satisfy the first and third conditions. The contact points 13 are arranged in the portions closer to the contact points 12 at the portions, which are not end portions of the conductive layer 11, for example, within an allowable range, which is determined every package.

The package of Figs. 11A and 11B is structured to satisfy all first to third conditions. More specifically, the distance C_1 between the adjacent two contact points 12 is 3/8 or less of the shortest distance h from one contact point of the inner lead to one contact point of the outer lead. Similarly, the distance C_2 between the adjacent two contact points 13 is 3/8 or less of the shortest distance h from one contact point of the inner lead to one contact point of the outer lead. The number of contact points 12 is equal to that of contact points 13.

Similar to the package of Figs. 10A and 10B, the package of Figs. 12A and 12B is structured to satisfy the first to third conditions. The contact points 13 are arranged in the portions closer to the contact points 12 at the portions, which are not end portions of the conductive layer 11, for example, within an allowable range, which is determined every package. In the packages of Figs. 13A to 16A and 13B to 16B, the conductive layer 11 is formed of four insulated parts. As a result, since each part does not influence the other parts, the uniformity of the distribution of current density of each part can be improved. In the package of Fig. 13A, the conductive layer 11 of Fig. 4A is formed of four parts. In the package of Fig. 13B, the conductive layer 11 of Fig. 4B is formed of four parts.

In the package of Fig. 14A, the conductive layer 11 of Fig. 6A is formed of four parts. In the package of Fig. 14B, the conductive layer 11 of Fig. 6B is formed of four parts. In the package of Fig. 15A, the conductive layer 11 of Fig. 7A is formed of four parts. In the package of Fig. 15B, the conductive layer 11 of Fig. 7B is formed of four parts. In the package of Fig. 16A, the conductive layer 11 of Fig. 8A is formed of four parts. In the package of Fig. 16B, the conductive layer 11 of Fig. 8B is formed of four parts.

Fig. 17 shows a conductive layer for power voltage V_{DD} of the ceramic flat package in which lead pitch P_1 is 25 [mil] and the number of leads is 300 or more. The distance C_1 between the adjacent two contact points 12 is set to 3/8 or less of the shortest distance h from one contact point of the inner lead to one contact point of the outer lead. Similarly, the distance C_2 between the adjacent two contact points 13 is set to 3/8 or less of the shortest distance h from one contact point of the inner lead to one contact point of the outer lead. The number of contact points 12 is equal to that of contact points 13.

Fig. 18 shows a conductive layer for power voltage V_{DD} of the ceramic pin grid array package in which lead pitch P_2 is 50 [mil] and the number of pins is 300 or more. The distance C_1 between the adjacent two contact points 12 is set to 3/8 or less of the shortest distance h from one contact point of the inner lead to one contact point of the outer lead. Similarly, the distance C_2 between the adjacent two contact points 13 is set to 3/8 or less of the shortest distance h from one contact point of the inner lead to one contact point of the outer lead. The number of contact points 12 is equal to that of contact points 13. The contact points 13 are arranged at the portions other than the end portions of the conductive layer 11, such as central portion of the conductive layer.

According to the semiconductor devices of Figs. 17 and 18, since the potential distribution is symmetrized, the distribution of current density can be uniformed, and the simultaneous switching noise of the package having a large number of pins can be reduced.

In the above embodiments, the distance C_1 between contact points 12 is set to be, for example, less than 100 [mil], and the distance C_2 between contact points 13 is set to be, for example, less than 100 [mil]. Each contact point 12 of the inner lead includes a via hole to be connected to an inner bonding pad or a bonding pad and a contact point between a bonding wire or TAB and the conductive layer. Each contact point 13 of the outer lead includes an outer pin of the package, a contact point between an outer lead of the package and the conductive layer, a via hole to be connected to the pin or the lead.

The conductive layer 11 can be formed of conductive material such as copper and tungsten. Regarding the conductive layer 11, the flat plate-like, mesh, layered, or thin-layer conductive layer may be used. Regarding the shape, a square or rectangular conductive layer can be considered. According to the package of the present invention, in particular, if the frequency of the output signal in the output buffer is 50 [MHz] or more (≧), delay of the output signal can be improved.

Table 1 shows the technical advantage of the present invention. According to the package of the present invention, as compared with the conventional package, the conductor resistance and inductance can be reduced by 20% or more, and simultaneous switching noise can be reduced. In Table 1, the conductive layer of Fig. 4 is used in the package of the present invention and the conductive layer of Fig. 1 is used in the conventional package.

Table 1

	Conventional Package	Package of Present Invention
Resistance [mΩ]	17.3	16.4
Inductance [nH]	5.01	3.80

Claims

1. A multilayer package, comprising:
   a semiconductor device (14);
   a conductive layer (11) applying a power voltage V_{DD} or a ground voltage V_{SS} to said semiconductor device;
   a plurality of inner leads (5) having one end connected to said conductive layer at the inner portion of said conductive layer and other end connected to said semiconductor device; and
   a plurality of outer leads (4) having one end connected to said conductive layer at the outer portion of said conductive layer and other end connected to said semiconductor device, wherein a first contact point between said conductive layer and each inner lead and a second contact point between said conductive layer and each outer lead are arranged to satisfy at least the following relationship:
   both C_1/h and C_2/h are 3/8 or less where a distance between adjacent two first contact points is C_1 and a distance between adjacent two second contact points is C_2, and the shortest distance from the first contact point to the second contact point is h.

2. The multilayer package according to claim 1, characterized in that the number of said first contact points is equal to that of said second contact points.

3. The multilayer package according to claim 1, characterized in that one end of each inner lead is connected to said conductive layer at one end portion of the inside of said conductive layer.

4. The multilayer package according to claim 1, characterized in that one end of each outer lead is connected to said conductive layer at one end portion of the outside of said conductive layer.

5. The multilayer package according to claim 1, characterized in that one end of each outer lead is connected to said conductive layer at a position where said one end extends inside by a predetermined distance from the end portion of the outside of said conductive layer.

6. The multilayer package according to claim 1, characterized in that said conductive layer is formed of a plate-like insulating substrate and a conductive film formed on said insulating substrate.

7. The multilayer package according to claim 6, characterized in that said plate-like insulating substrate and conductive film are shaped square.

8. The multilayer package according to claim 7, characterized in that a semiconductor device is mounted on a central portion of said conductive film.

9. The multilayer package according to claim 6, characterized in that said plate-like insulating substrate and conductive film are shaped square and have square holes in their central portions.

10. The multilayer package according to claim 1, characterized in that said conductive layer is formed of a plate-like conductive member.

11. The multilayer package according to claim 10, characterized in that said plate-like conductive member is shaped square.

12. The multilayer package according to claim 10, characterized in that a semiconductor device is mounted on a central portion of said conductive member.

13. The multilayer package according to claim 10, characterized in that said plate-like conductive member is shaped square and has square holes in its central portions.

14. The multilayer package according to claim 1, characterized in that said conductive layer is formed of a plurality of parts, and each part is formed around said semicon ductor device.

15. The multilayer package according to claim 1, characterized in that said multilayer package has 300 or more outer leads.

16. The multilayer package according to claim 1, characterized in that said multilayer package is used in a case where a frequency of an output signal in an output buffer formed in said semiconductor device is 50 [MHz] or more.

17. The multilayer package according to claim 1, characterized in that one of said first contact point and one of said second contact point are paired, and said first and second contact points are opposed to each other with the shortest distance.

18. The multilayer package according to claim 1, characterized in that said respective parts of said conductive layer are insulated from each other.

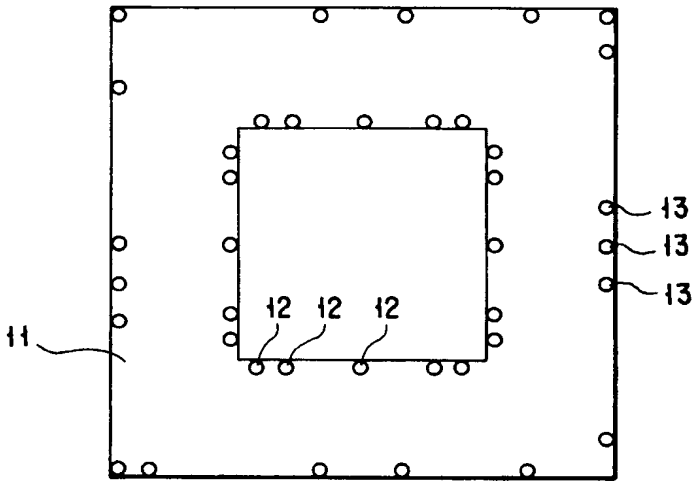


FIG. 1

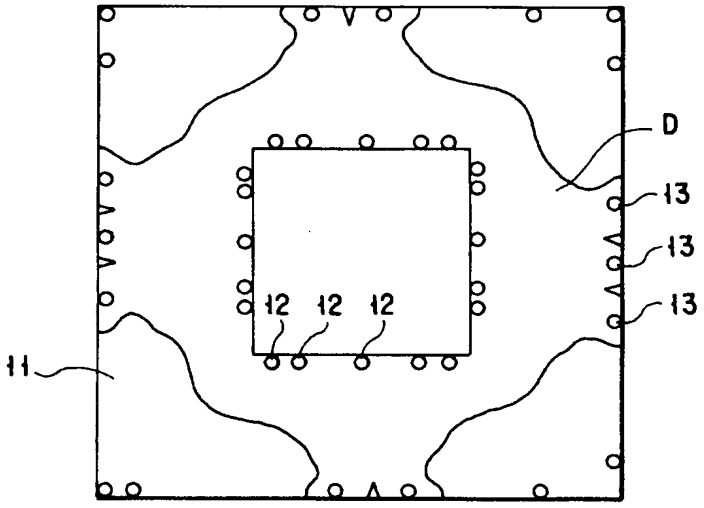


FIG. 2

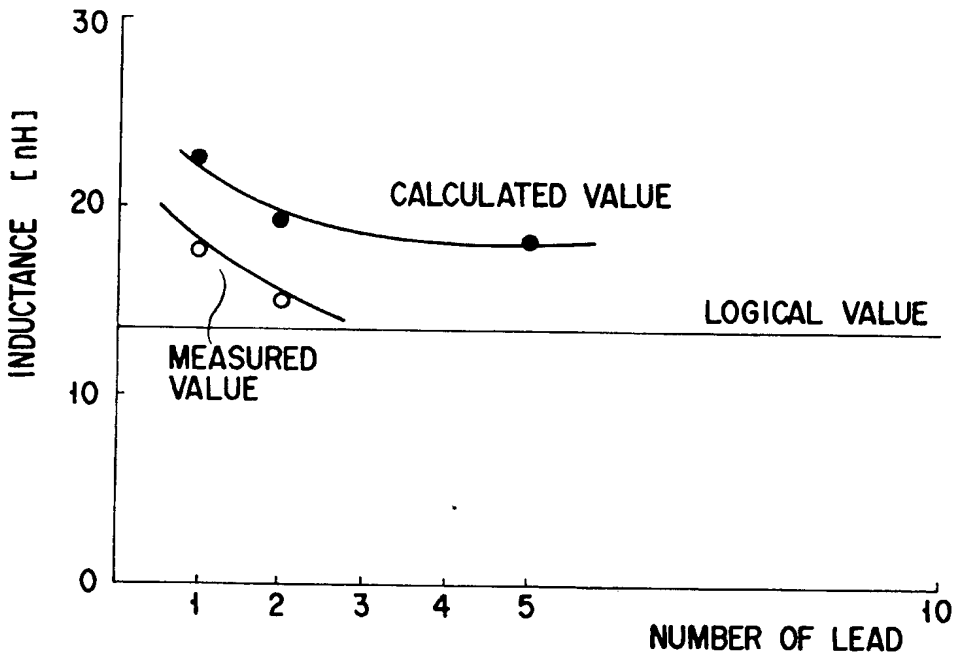

30
20
10
0
INDUCTANCE [nH]
CALCULATED VALUE
LOGICAL VALUE
MEASURED VALUE
1
2
3
4
5
10
NUMBER OF LEAD

FIG. 3

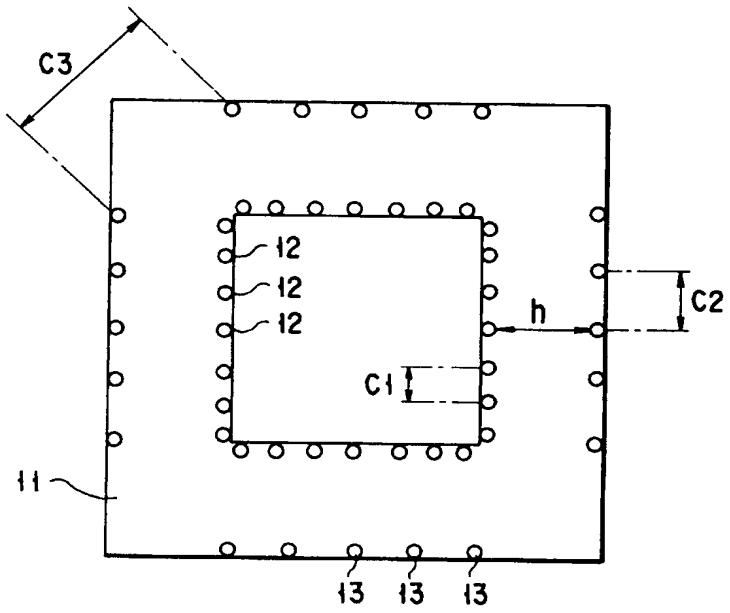


FIG. 4A

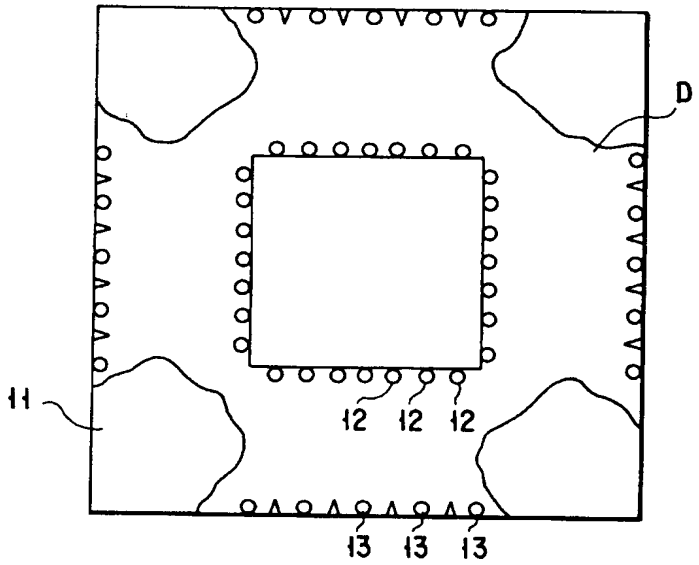


FIG. 5

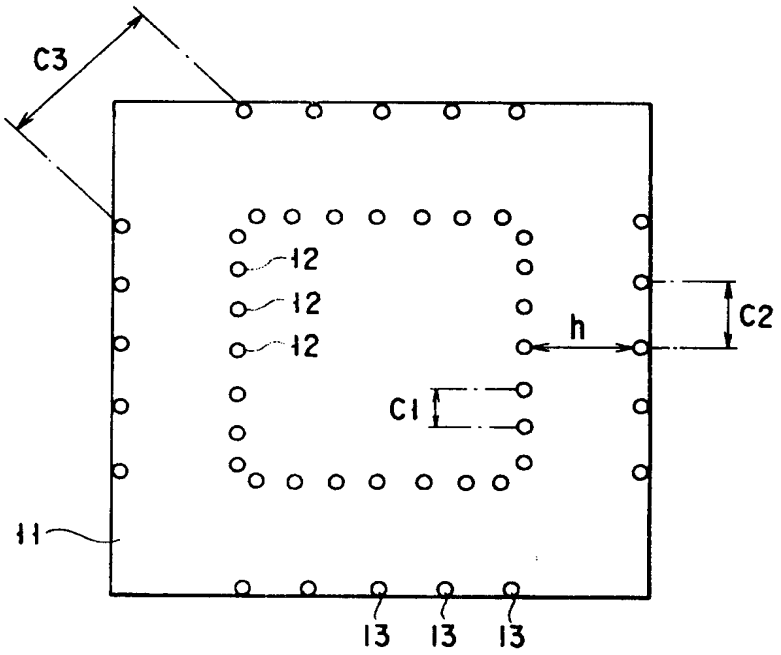
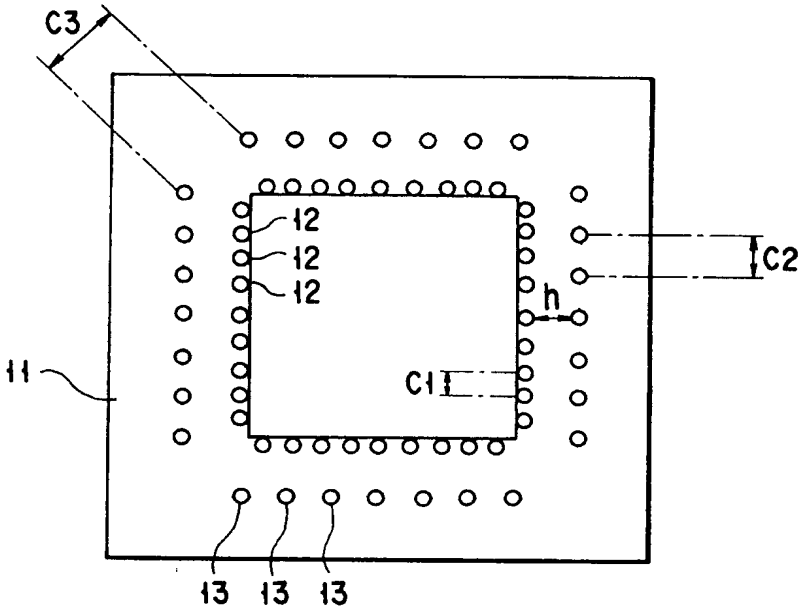
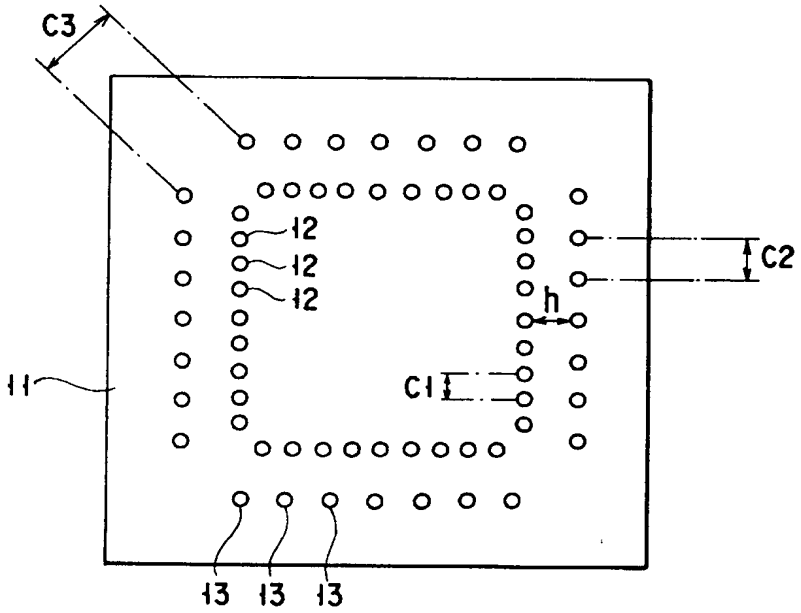


FIG. 4B



F I G. 6A



F I G. 6B

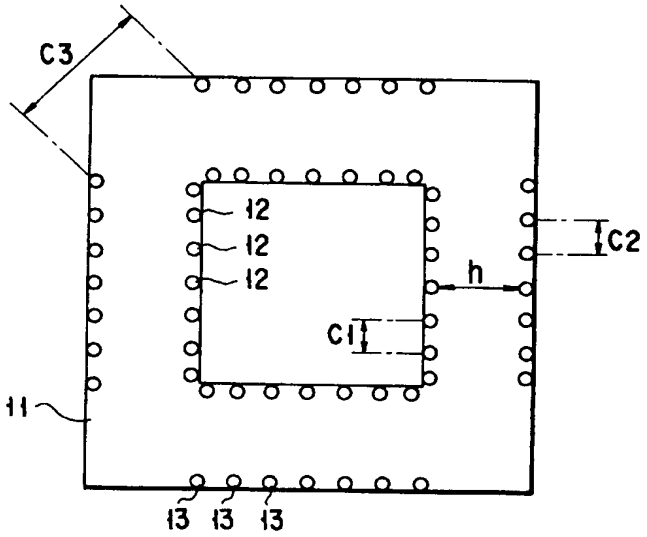


FIG. 7A

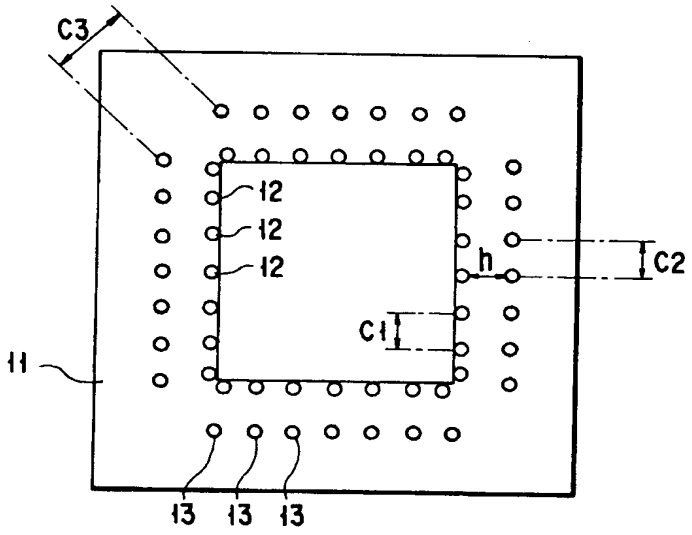


FIG. 8A

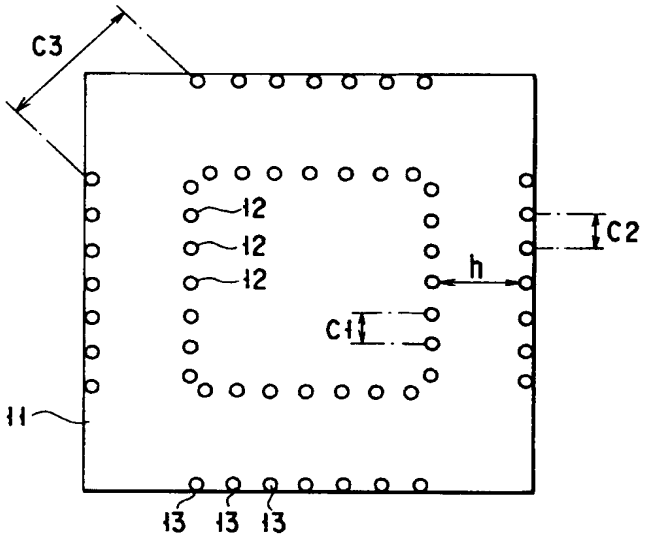


FIG. 7B

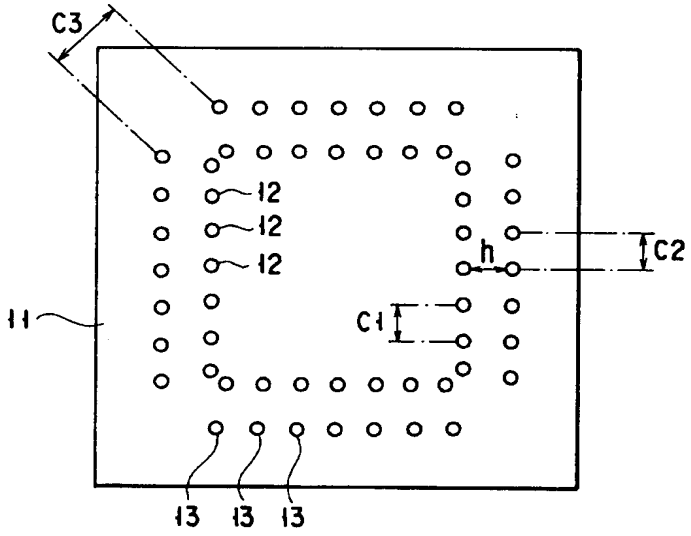
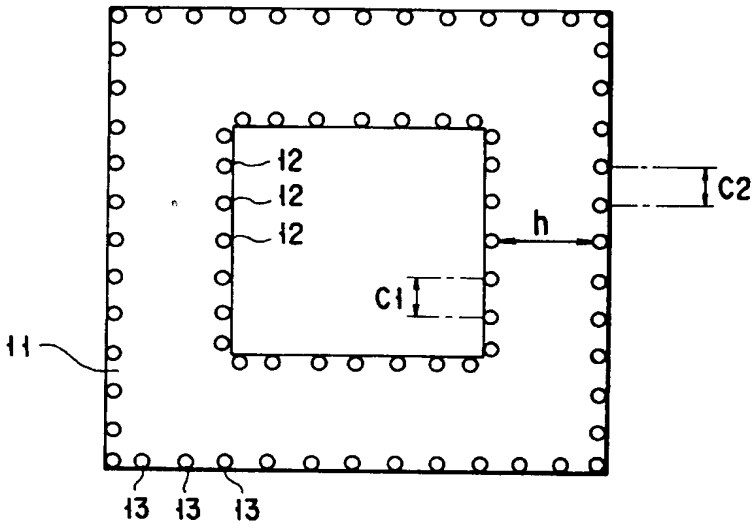
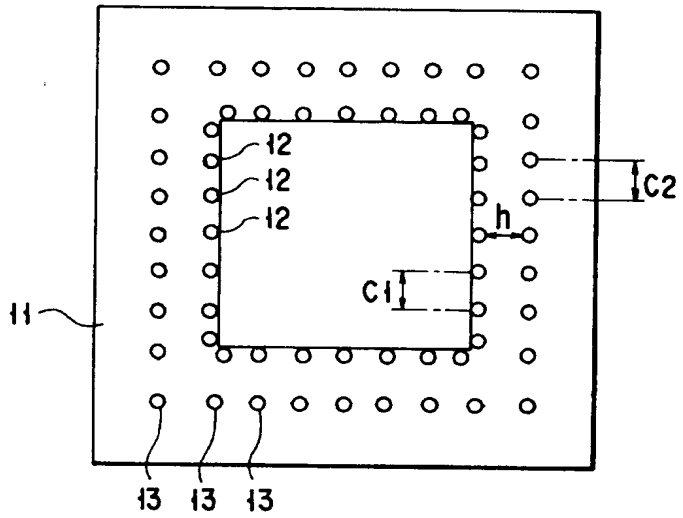


FIG. 8B



F I G. 9A



F I G. 10A

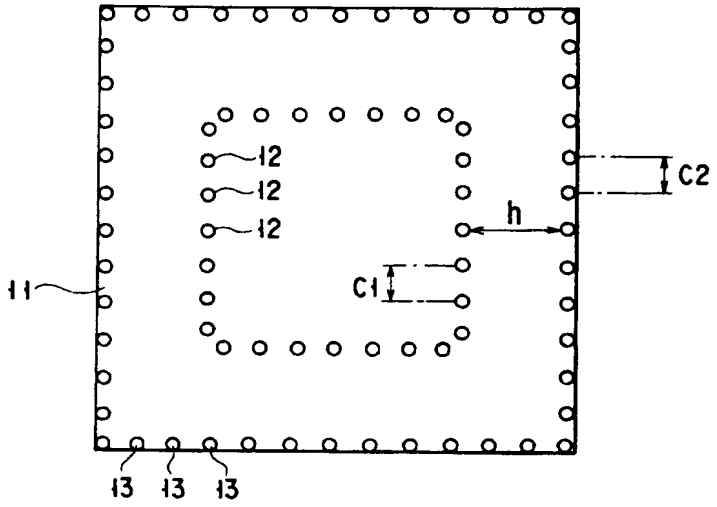


FIG. 9B

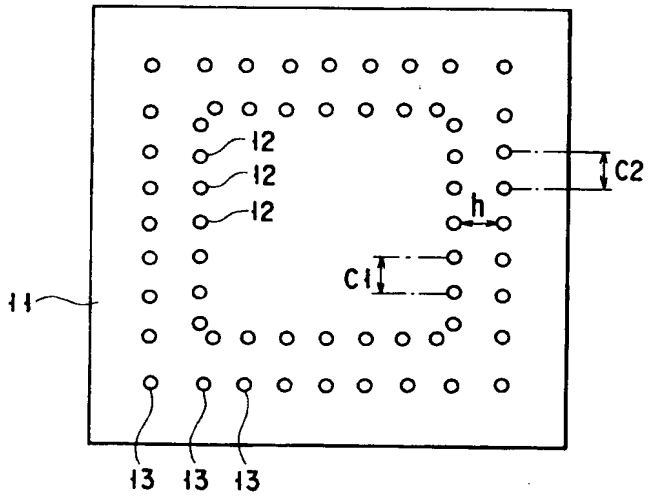


FIG. 10B

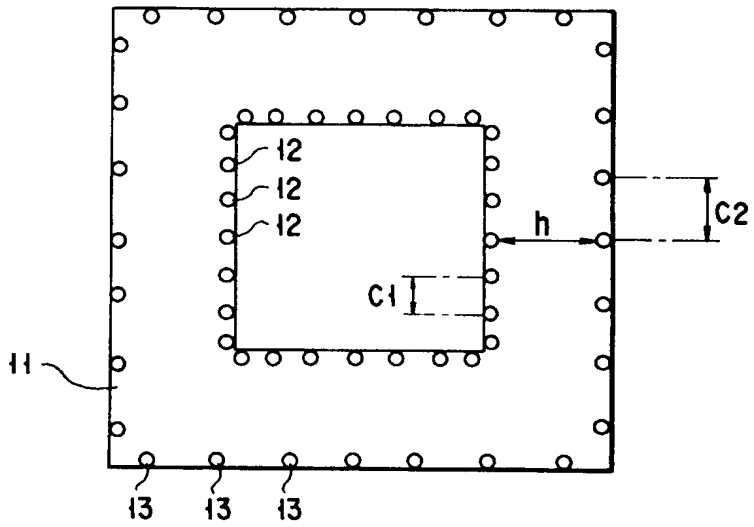


FIG. 11A

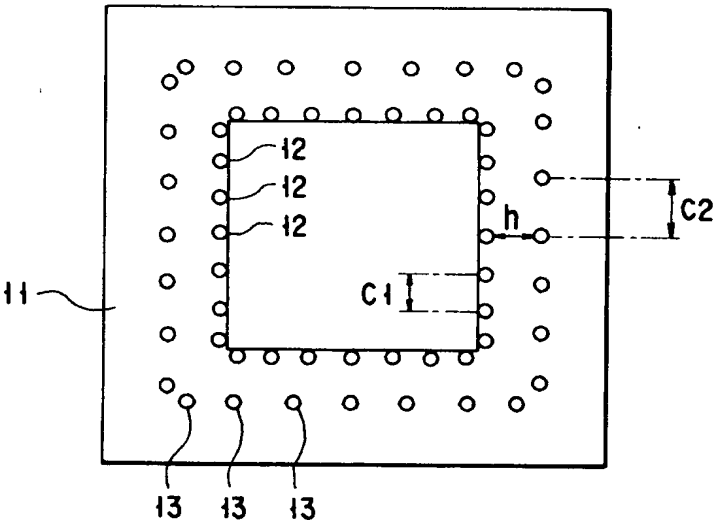


FIG. 12A

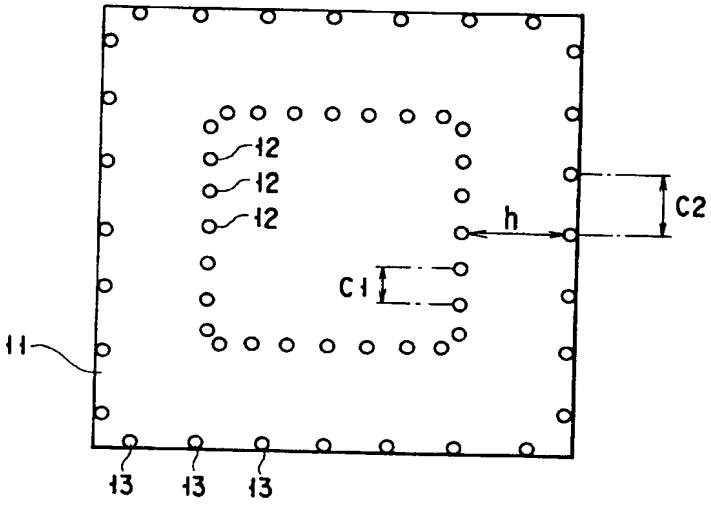


FIG. 11B

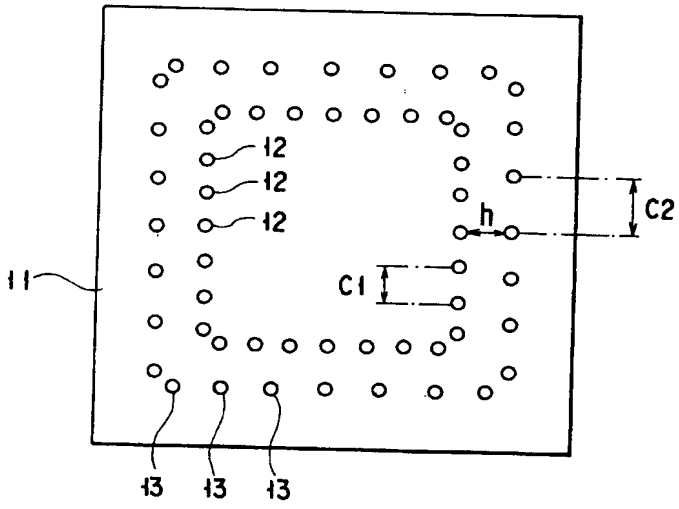


FIG. 12B

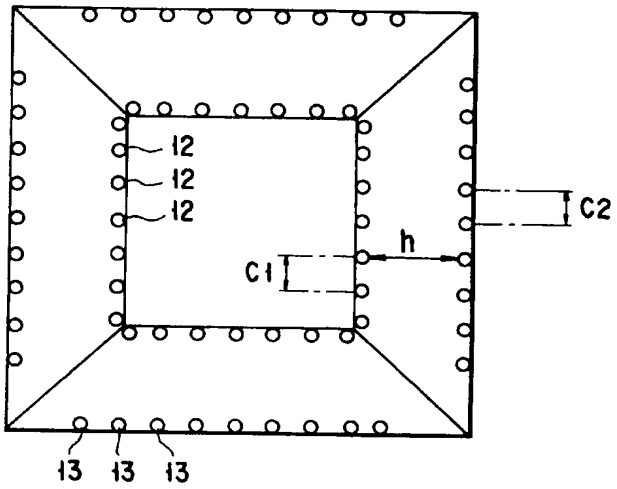


FIG. 13A

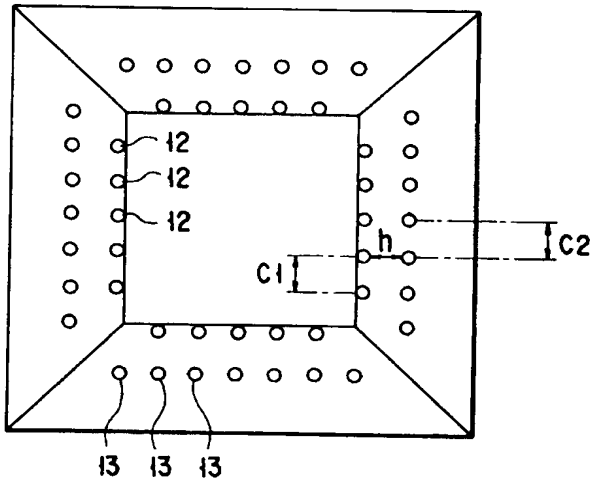


FIG. 14A

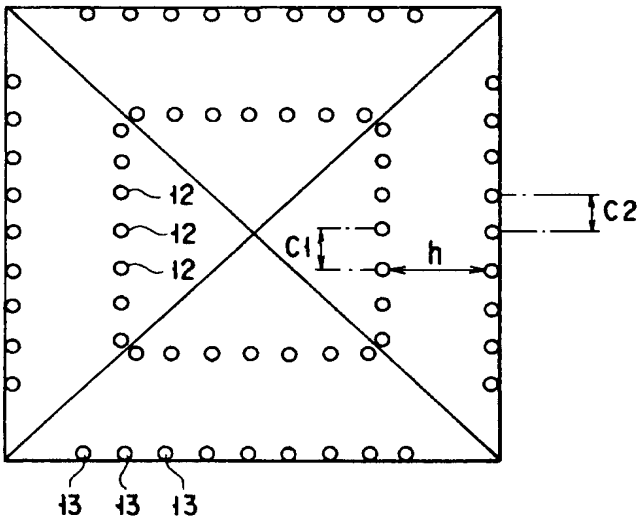


FIG. 13B

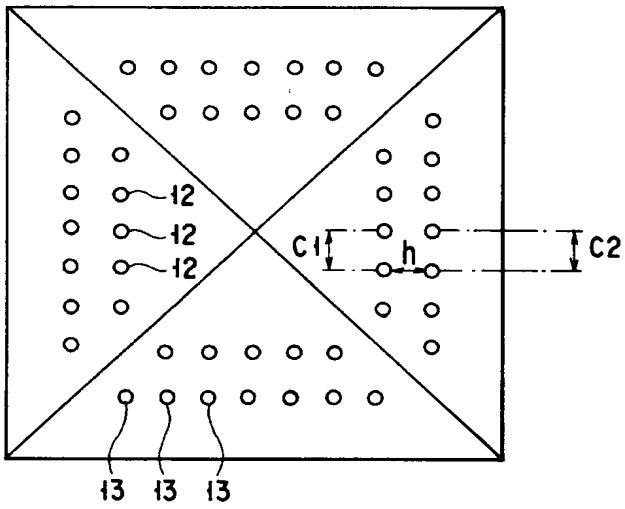


FIG. 14B

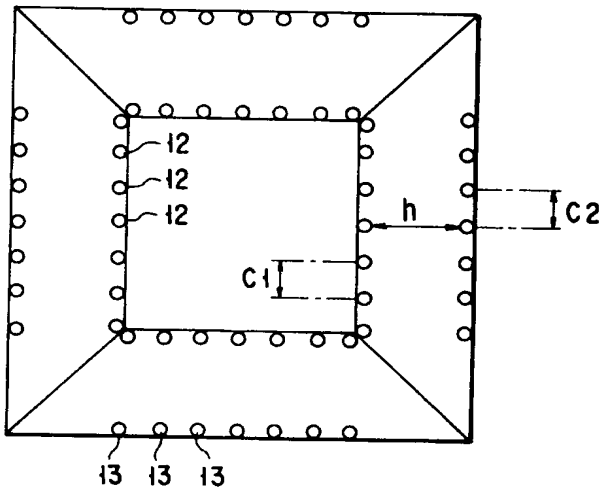


FIG. 15A

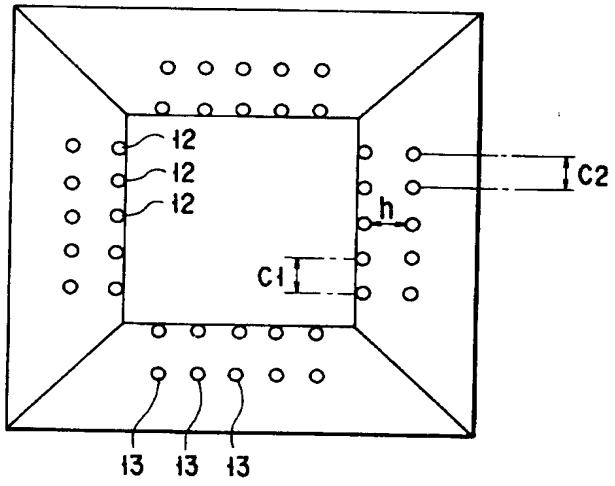
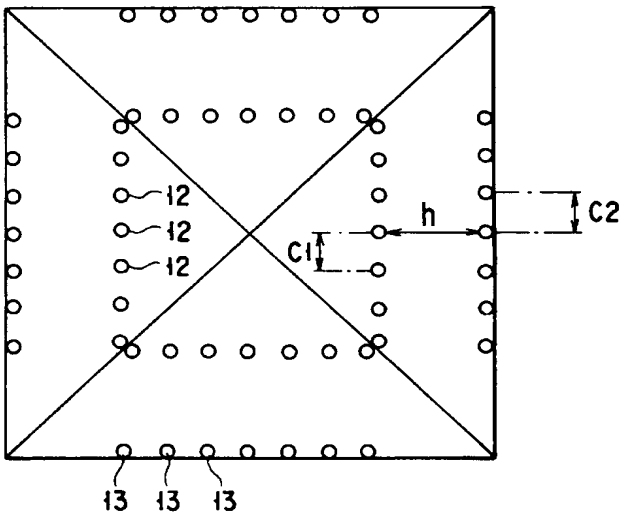
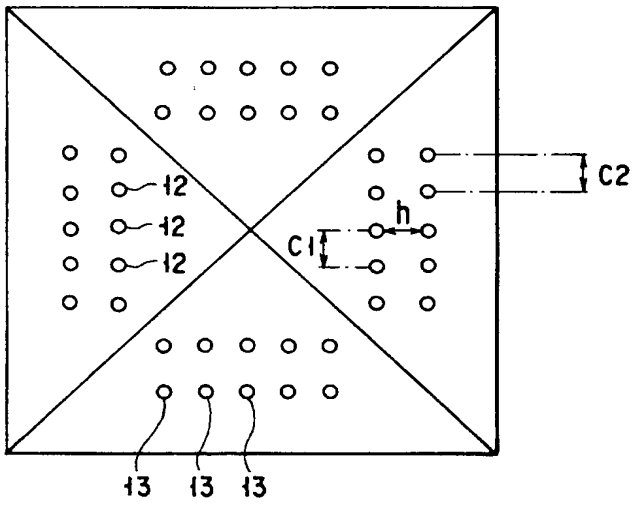


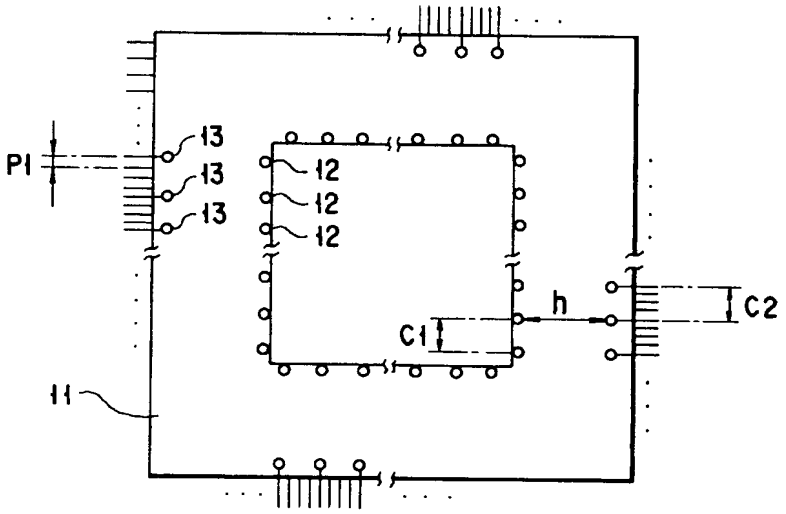
FIG. 16A



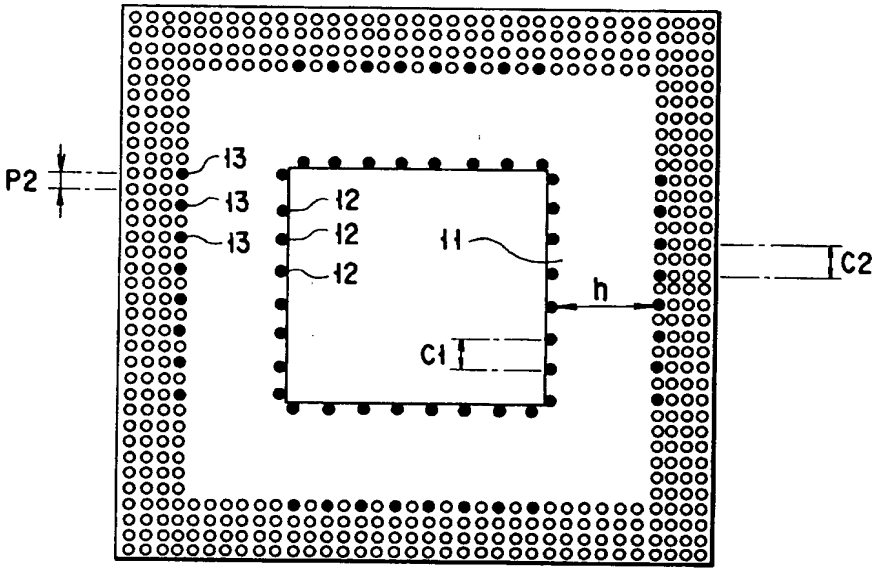
F I G. 15B



F I G. 16B



F I G. 17



F I G. 18

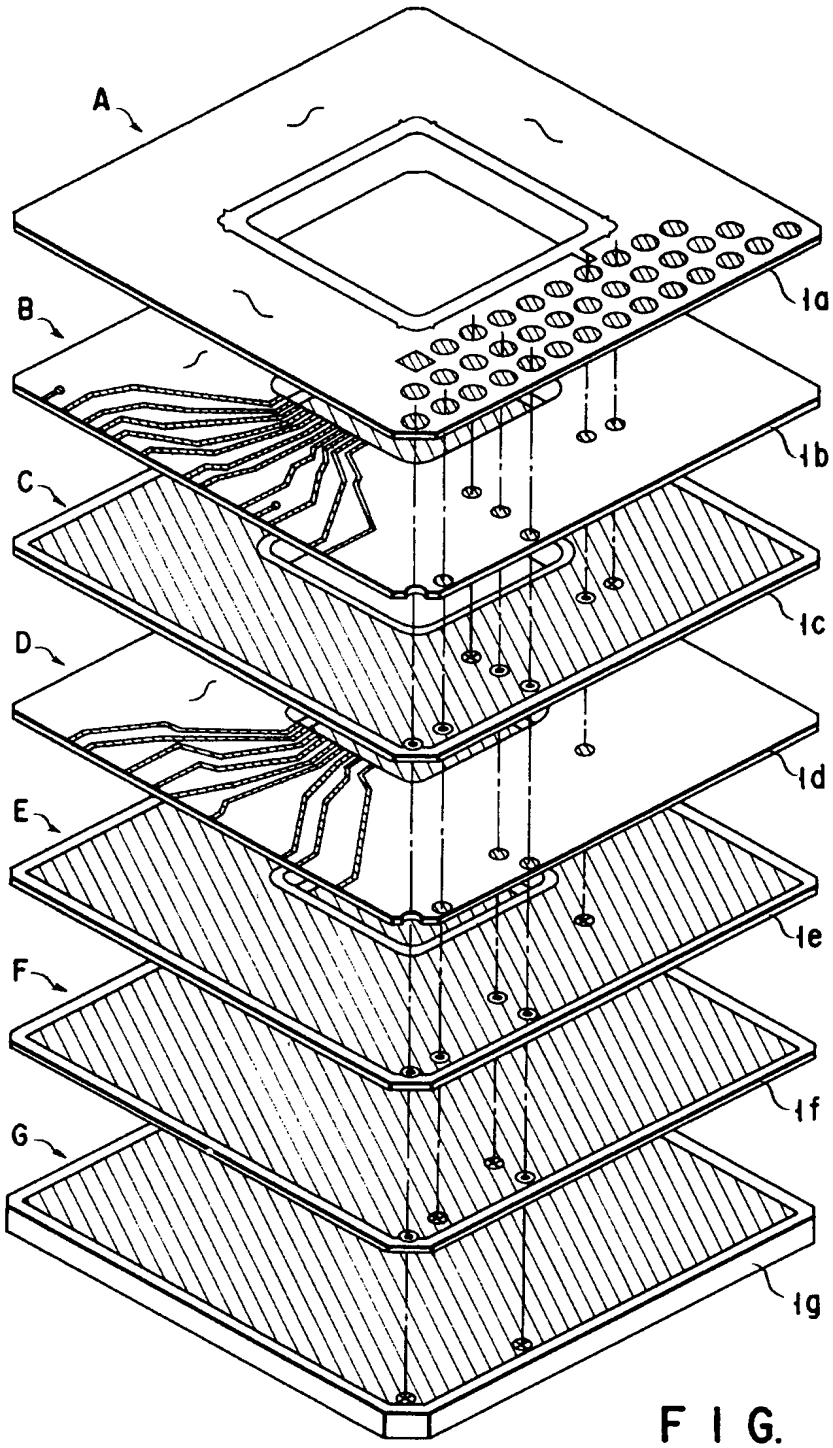
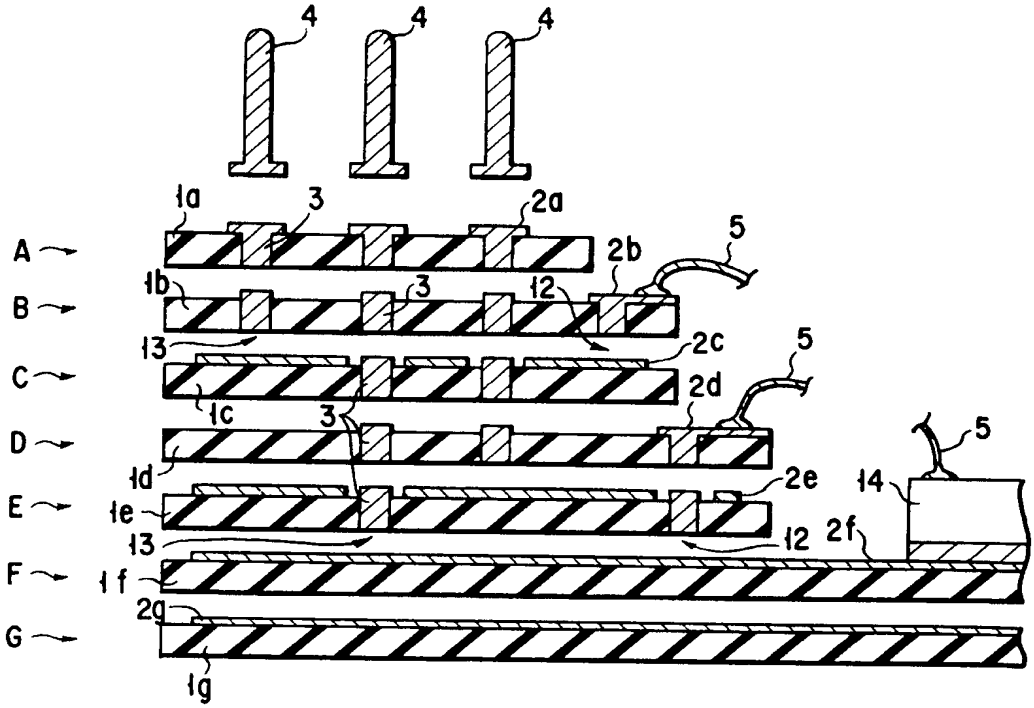


FIG. 19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C
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1f
2g
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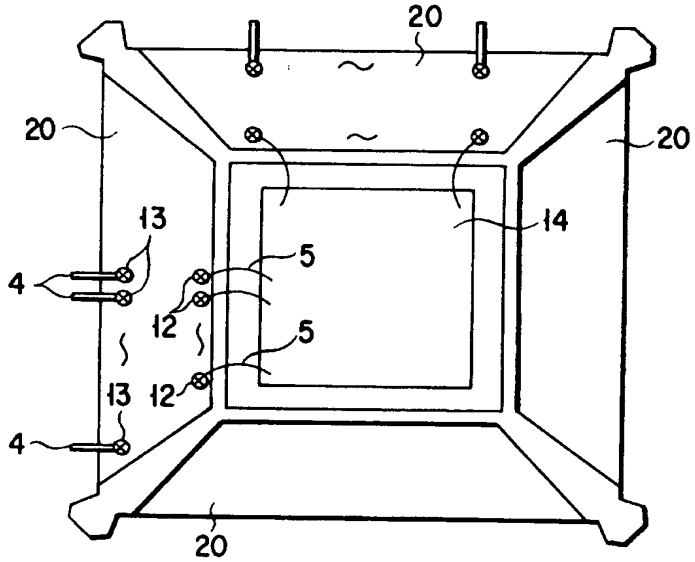
1g

F I G. 20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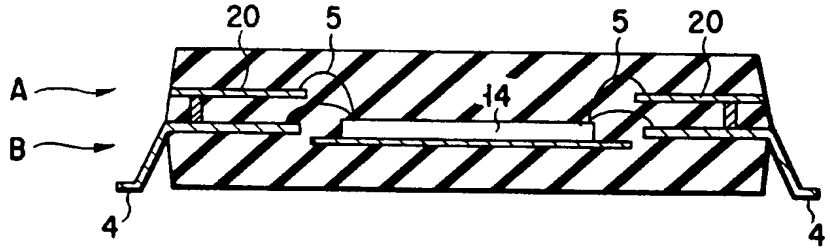
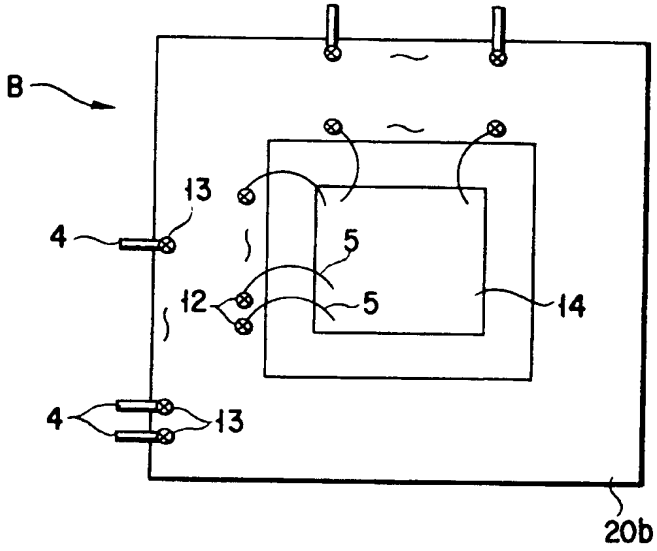
F I G. 21



F I G. 22



F I G. 23

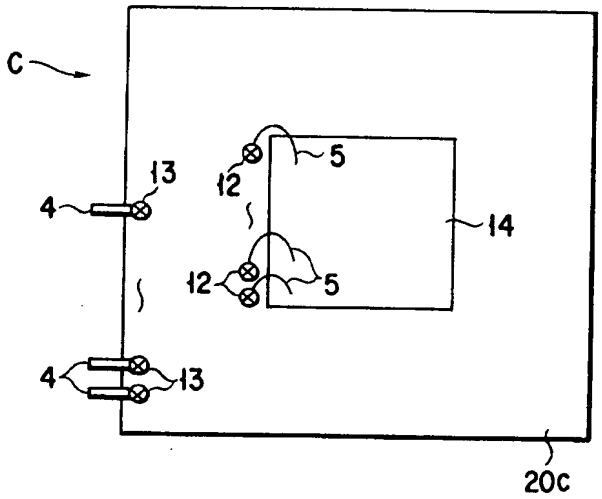


FIG. 24

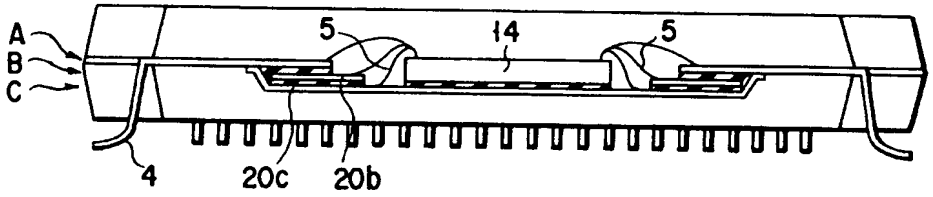


FIG. 25